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Development of COTS ADC SEE test system for the ATLAS LAr calorimeter upgrade*

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Commercial off-the-shelf (COTS) ADCs (analog-to-digital converters) that are radiation-tolerant, high speed, high density and low power will be used in upgrading the LAr (liquid argon) calorimeter front end (FE) trigger readout electronics. Total ionization dose (TID) and single event effect (SEE) of the COTS ADCs should be characterized. In our initial TID test, 17 COTS ADCs from different manufacturers with dynamic range and sampling rate meeting requirements of the FE electronics were checked, and the ADS5272 of Texas Instruments (TI) was the best performer of all. Another interesting feature of ADS5272 is its 6.5 clock cycles latency, which is the shortest of all the 17 candidates. Based on the TID performance, we designed an SEE evaluation system for ADS5272, which allows us to further assess its radiation tolerance. In this paper, we present a detailed design of ADS5272 SEE evaluation system and show the effectiveness of this system while evaluating ADS5272 SEE characteristics in multiple irradiation tests. According to TID and SEE test results, ADS5272 was chosen to be implemented in the full-size LAr Trigger Digitizer Board (LTDB) demonstrator, which will be installed on ATLAS calorimeter during the 2014 Long Shutdown 1 (LS1).

Keywords: COTS ADC, Total ionization dose, Single event effect, Single event upset, Single event functional interrupt

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I. INTRODUCTION

At LHC (Large Hadron Collider), CERN, the ATLAS LAr calorimeter upgrade project is proposed to enhance physics experiment in the high-luminosity environment foreseen in the next 10 years [1]. In order to provide higher-granularity, higher-resolution and longitudinal shower information from the calorimeter to level-1 trigger processors in this upgrade, new LAr calorimeter trigger readout electronics should be designed, built and installed. Compared to the existing readout cell "trigger tower", the new readout element referred as Super Cell [1], which is a 10-fold finer granularity scheme, also provides additional information and more powerful tools to the Level-1 trigger feature extraction. Also, the digitization precision of the Super Cell signals is improved by at least a factor of 4 compared to the existing Level-1 system by optimizing the quantization scale and the dynamic range of the digitizers. These upgrades will be essential to extend the physics potential at higher instantaneous luminosities and more severe pileup conditions expected after Phase-I and Phase-II upgrades of the LHC.In the Phase-I upgrade, $\sim$ 40,000 channels of Super Cell signals will be digitized at the front end LTDB, and data will be streamed out to the back end DPS (digital processing system). A radiation tolerant ADC is required for signal digitization in the front end electronics. The LAr collaboration has prepared two technological routes: custom ASIC (application-specific integrated circuit) ADC development and COTS ADC evaluation. Two custom ASIC ADCs are under different stages of prototyping developments. However, given the uncertainty in the development cycle and costs associated with a custom chip design, an extensive study has been conducted for a COTS option that meets both electrical and radiation requirements. Previous studies on the radiation sensitivity to many COTS parts can inform component decisions appropriate for our design. Good experience can be found in Reference [2–5].

In this paper, the TI COTS ADC, ADS5272 [6], is chosen as a good candidate for use in the LAr calorimeter electronics upgrade. Its electrical features include: maximum sampling rate, 65 *MSPS* (million samples per second); dynamic range, 12 bit; resolution, 11.5 ENOB (effective number of bits), latency, 162.5 ns (6.5 clock cycles); and power consumption per channel, 113 mW. These parameters meet the digitization requirements [1] of the LAr calorimeter upgrade, and therefore a test program was developed to study irradiation properties of ADS5272. The outline of this paper is organized as follows. In Section II, we show the *TID* radiation effects of 17 COTS ADCs. In Section III, we discuss the detailed development of the ADS5272 SEE evaluation system. In Section IV, we use our evaluation system to characterize the ADS5272 SEE radiation tolerance. Finally we conclude this paper in Section V.

II. TOTAL IONIZATION DOSE (TID) IRRADIATION TEST

Long-term exposure to ionizing radiation can cause parametric degradation and ultimately functional failure in elec-

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TABLE 1. Diagram TID test results of COTS ADCs in June 2012

COTS ADC	Dynamic Range (bit)	*MSPS*	Analog input span (V_{p-p})	Channels per chip	Ptotal per channel (mW)	Vendor	*TID* (kGy(Si))
AD9265-80	16	80	2	1	210	ADI	∼ 2.2
AD9268-80	16	80	2	2	190	ADI	∼ 1.6
AD9268-40	16	40	2	2	61	ADI	∼ 1.2
AD9650-65	16	65	2.7	2	175	ADI	∼ 1.7
AD9253-125	14	125	2	4	110	ADI	∼ 1.1
LTC2204	16	40	2.25	1	480	Linear	∼ 1.8
LTC2173-14	14	80	2	4	94	Linear	∼ 1.1
LTC123	16	80	2	2	125	Linear	∼ 1.0
ADS4245	14	125	2	2	140	TI	∼ 2.4
ADS6445	14	125	2	4	320	TI	∼ 2.1
ADS5282	12	65	2	8	77	TI	∼ 4.6
ADS4245	16	100	4	4	280	TI	∼ 21.0
ADS4245	14	80	2	8	77	TI	∼ 10.7
ADS4245	12	80	2	8	66	TI	∼ 10.6
ADS4245	12	65	2.03	8	125	TI	∼ 88.0
HMCAD1520	14	105	2	4	133	Hittite	∼ 23.0
HMCAD1102	12	80	2	8	59	Hittite	∼ 17.3

tronic devices. The damage occurs via electron-hole pair production, transport and trapping in the dielectric and interface regions.

To examine the effect of this issue on the COTS ADC, we performed *TID* tests on the ^{60}Co gamma irradiation facility for solid state physics at Brookhaven National Laboratory (BNL). The test flow is shown in Fig. 1 and the results are shown in Table 1 [7].

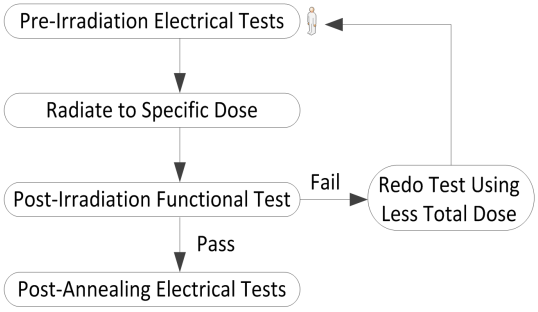

Fig. 1. Diagram of *TID* test flow.

Of the six ADCs which withstood doses of over 1 Mrad (Si) in the bottom six rows in Table 1, the ADS5272 is the best performer–88 kGy (Si). See Fig. 2(a) for its test results. Also, two ADS5272 samples were annealed at ∼ 85 °C after 24 kGy (Si) *TID* test. After annealing, both ADCs recovered to their original characteristics. Fig. 2(b) shows the analog and digital power consumption of Sample 2 before and after annealing.

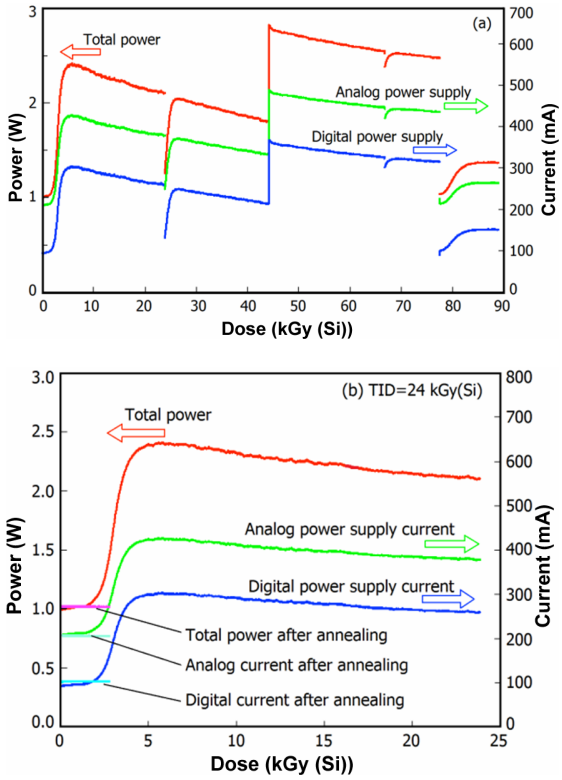

Fig. 2. (Color online) Power consumption of ADS5272 #2 in 88 kGy(Si) test (a) and its recovery after 24 kGy(Si) test and annealing at 85 °C (b).

III. SINGLE EVENT RADIATION EFFECTS

Based on the test results in Section II, an evaluation system for ADS5272 was established to characterize its single event effects. This system consists of three parts:

1) Hardware, an ADS5272 test board (Fig. 3) is custom built for SEE test.

2) Firmware, we implement firmware in Virtex-6 FPGA on ML605 [8, 9], which is generally responsible for acquiring data from the ADC, and controlling and monitoring it.

3) Software, it is developed in MATLAB GUI, which com-

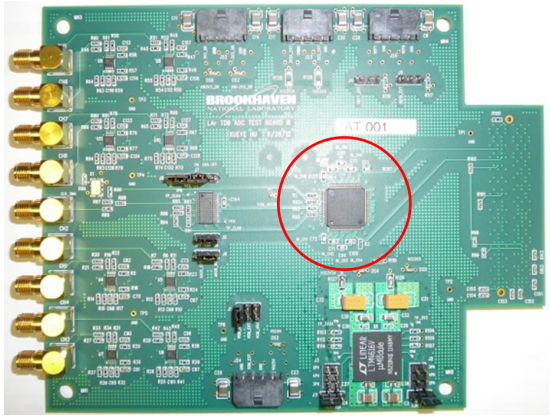

Fig. 3. (Color online) The ADS5272 test board.

municates with ML605 through Ethernet connection, sending configuration information and saving data for analysis in the case of a SEE.

A. Design of ADS5272 test board

SMA connectors were chosen as the input connectors for the ADS5272 test board. The output connector is a Samtec FMC (FPGA Mezzanine Card) HPC connector. This makes the ADS5272 test board easy to attach to the ML605. In order to make the input signals match with the differential full-scale input voltage range of ADS5272, an ADC driver was added in the analog signal chain. The ADC driver is ADI AD8138 (Fig. 4), which was qualified up to 5 kGy *TID*. The AD8138 output and ADS5272 input are DC coupled with RC low pass filtering to improve the signal-to-noise ratio (*SNR*).

The clock scheme for the ADS5272 has three options: SMA input clock, FPGA differential output clock and on board oscillator. ADS5272 needs a LVTTL clock, so a Maxim MAX9160 was chosen as clock fan out driver for all clock input options, which had survived $\sim$ 150 kGy TID.

There are two power supplies: an external supply and an on board POL (Point-of-Load) DC-DC converter LTM4616 from Linear Technology. The external power supply is responsible for AD8138 power ± 3.3 V, ADS5272 analog power +3 V and digital power $+3$ V (contingency), ADS5272 reference voltage REFT $+1.95$ V and REFB $+0.95$ V, ADS5272 common-mode voltage $+1.45$ V, and LTM4616 input +5 V. The DC-DC converter LTM4616 can provide analog and digital power to the ADS5272. A detailed block diagram of the ADS5272 test board is depicted in Fig. 5. As required by the irradiation test, a clearance circle of 3 inches diameter is designated around the ADS5272 (Fig. 4), where no other active component is placed.

B. Development of firmware in Virtex-6

The firmware of the ADS5272 SEE test system is developed in a Virtex-6 FPGA, which mainly consists of a MicroBlaze (UBLZ) core system and the FPGA fabric logic. The block diagram is illustrated in Fig. 6. UBLZ is a 32 bit RISC (Reduced Instruction Set Computer) embedded processor soft core, which is generated to acquire data from the ADC and compare it with an LUT (Look-Up Table). Then, the data are buffered to DDR3 SDRAM for reading out through Gigabit Ethernet or USB. The FPGA fabric logic is comprised of five sub-function blocks: ADC logic block, LUT generator block, comparison & SEE detection block, NPI (Native Port Interface) data generator block and UBLZ IO bus interface (IF) block.

ADC logic block is mainly responsible for the following functions: 1) de-serialize ADC raw serial data from serial to parallel (S2P); 2) control and program ADC settings through a serial peripheral interface (SPI); 3) keep ADC bit clock 90 out-of-phase with respect to the data and frame clock through ADC sampling clock alignment (SCA). SCA function is realized through the adjustment of IODELAYE1 primitive of the FPGA according to associated SNR and noise floor plots.

The LUT generator basically aims to generate a programmable look up table via FPGA embedded block RAM resources. This look up table will be aligned and locked with the ADC waveform before the beam test starts. It is a critical preparation for comparison & SEE detection block.

Real time comparison of ADC data vs. LUT is done in the comparison & SEE detection block. This block can continuously check the difference between the ADC and LUT. When the difference is larger than the preset threshold, which is programmable, the case shall be deemed as an SEE event. An error flag will then be polled to initiate DDR3 transfer and an error counter will start counting.

The NPI data generator block provides logic to compose ADC & LUT data according to PLB (IBM CoreConnect®Tookit Processor Local Bus) timing and data structure rules. The NPI block sends data to the MPMC (Multi-Port Memory Controller) NPI interface. It also has a verification function to send user test patterns that is permitted by an enable signal (Verif_en) generated from UBLZ IO bus IF block.

The UBLZ IO bus IF block provides a read-write register interface, which is connected as a bridge to a UBLZ processor. It just leverages a simple user logic bus to decode a bunch of transactions. Write operations include transporting configuration information and delay tap values from MATLAB to ADC logic block, and updating the LUT according to the mean value of 100 samples calculated by MATLAB. It also sets the threshold to detect an SEE event and triggers the DDR3 test transfer as well. Read operations consist of getting values of the ADC registers and SEE error counter, examining SEE error flags and reviewing test patterns.

C. Software realized in MATLAB GUIDE

Software is built on the GUI panel (Fig. 7) with MATLAB GUIDE, which talks to the UBLZ system via TCP/IP server sockets.

MATLAB applications serve three principal functions. The

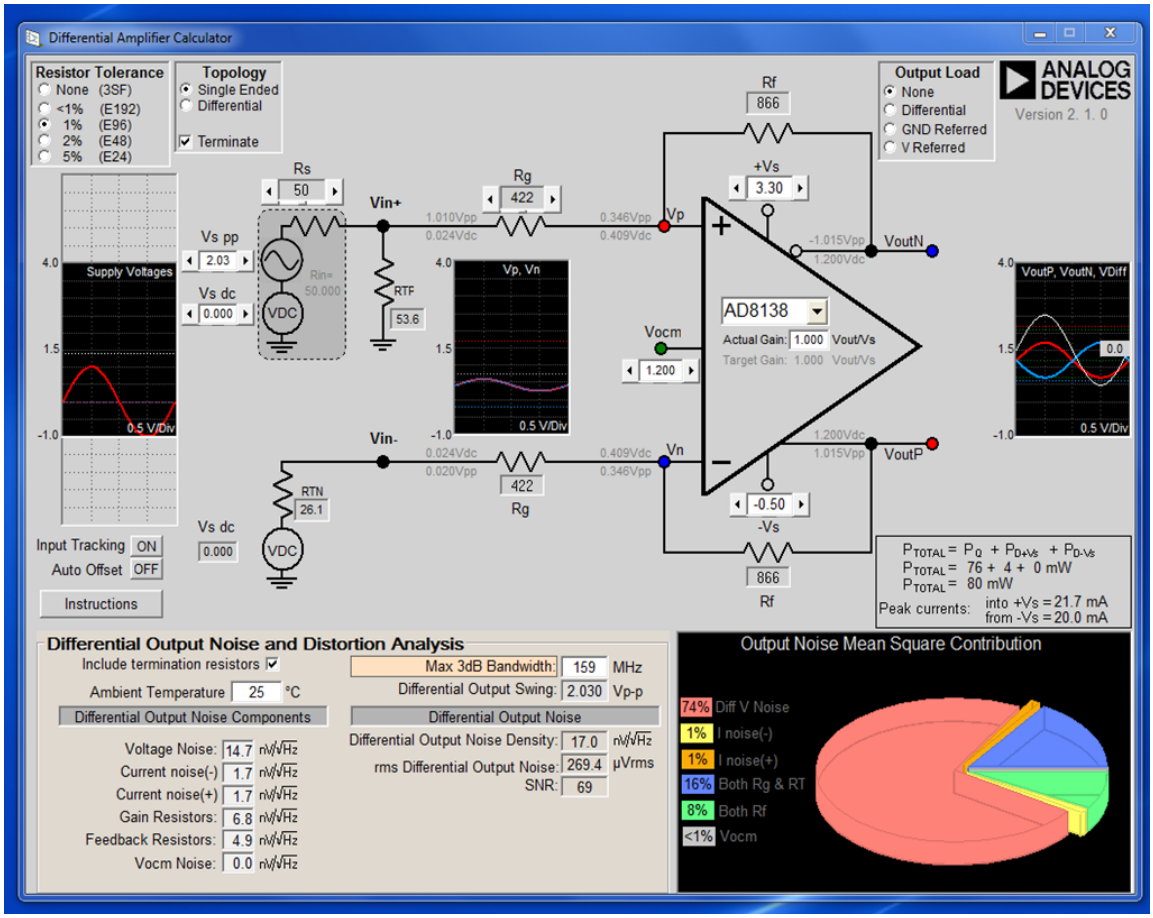

Fig. 4. (Color online) Simulation of AD8138 circuit.

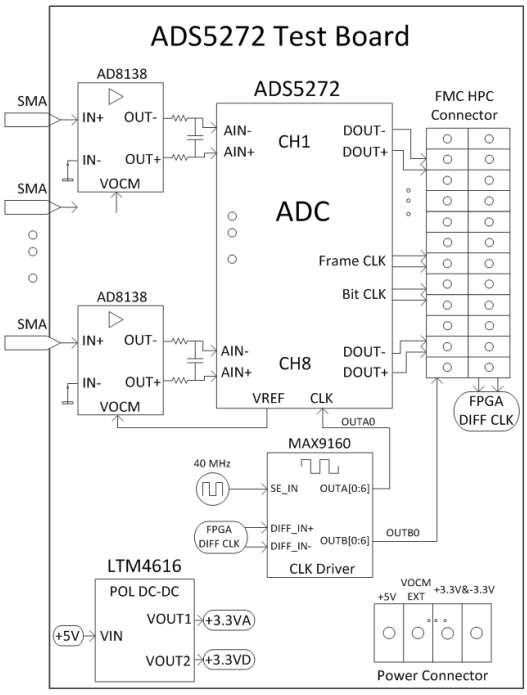

Fig. 5. Diagram of hardware development of SEE test system.

first function is calculation and analysis. MATLAB calculates the mean value and RMS of the difference between ADC and LUT with 100 samples, sends the mean value back to the firmware "LUT Generator" block to update and match the LUT with ADC data. MATLAB also performs FFT with ADC data to get the corresponding noise level and SNR (Signal Noise Ratio) plot. It will then round the mean value of all working delay taps to get the most appropriate value for ADC SCA.

The second function is a control "eyboard". All input control information is manipulated by MATLAB. This includes issuing ADC hardware reset, sending ADC SPI configuration bits, adjusting the LUT address value and offset value, triggering a DDR3 transfer, setting the SEE error threshold, manually injecting an error to SEE test system for simulation and so on.

The third function is remote "monitor". MATLAB can plot the ADC data vs. LUT in real time and display ADC register values on the GUI. Also, it monitors the voltage of the power supply and the amplitude of signal generator through Ethernet. This facilitates debugging and testing.

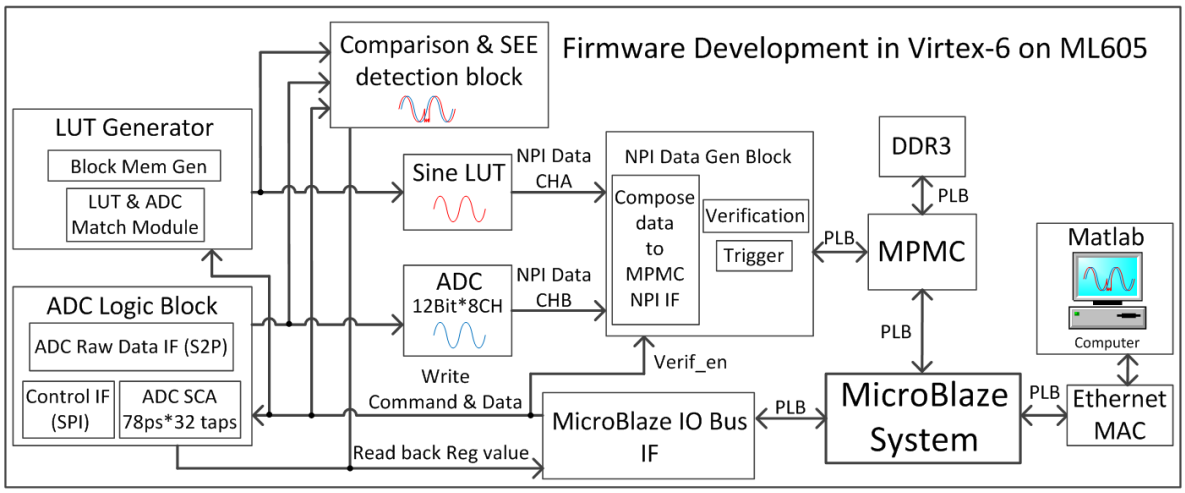

Fig. 6. (Color online) Diagram of firmware development of SEE test system.

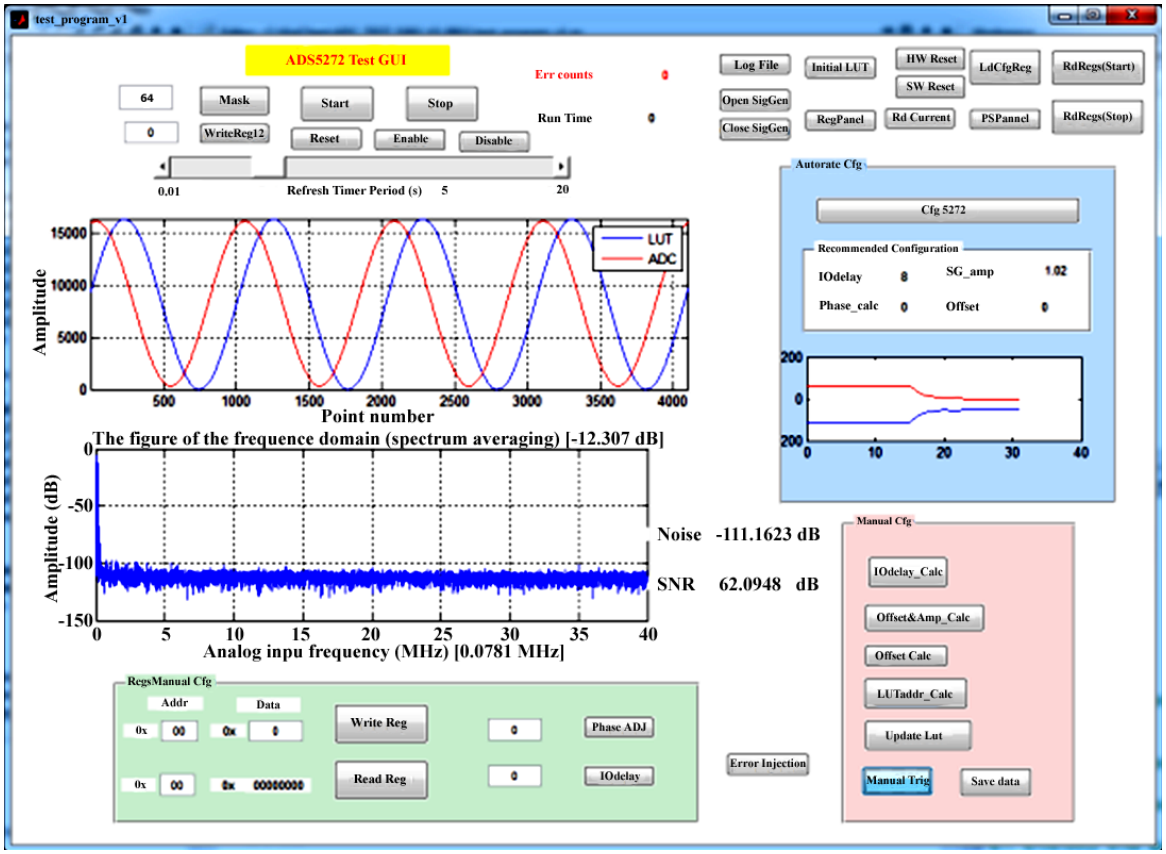

Fig. 7. (Color online) A picture of SEE software GUI panel.

IV. SEE TEST RESULTS

The ADS5272 SEE evaluation system has been successfully used in multiple irradiation tests. In October 2012, a test was performed at LANSCE WNR (Los Alamos, NM) with initial neutron beams in maximum energy of about 800 MeV. The neutron spectrum matches to what is expected at the position of ATLAS LAr electronics crate. The second test was done at IUCF, Bloomington, IN (see Section IV B) to illustrate the correctness and practicality of the ADS5272 SEE test system. Another test was conducted in Mass General Hospital (Boston, MA) with 216 MeV protons. The total SEU (single event upsets) cross section observed in these tests are consistent with each other.

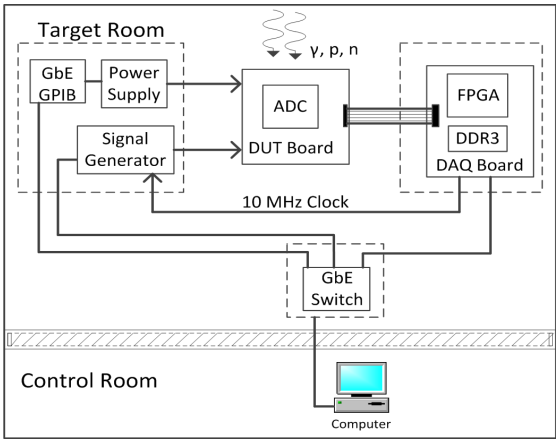

Fig. 8. (Color online) Diagram of SEE test setup.

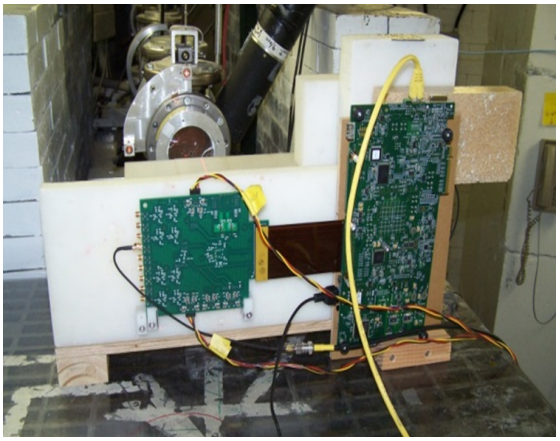

Fig. 9. (Color online) ADS5272 SEE test at IUCF.

A. Test setup

The beam tests described above shared similar test set up. We used a signal generator to inject a sine wave into ADS5272, which was running at $f_{\text{sample}} = 40$ MSPS. The frequency of the sine wave was about 40 kHz ($f_{\text{sample}}/2^{10}$) to ensure that enough samples were acquired for each cycle. The FPGA acquired ADC data and compared samples with the LUT in real time. Any deviation being larger than a preset threshold was flagged as an SEE event, and a record of $\sim$ 4 k samples was saved for posterior analysis. The system was synchronized by a 10 MHz clock, which was generated by the ML605 board. The test setup diagram is shown in Fig. 8 [7].

B. Proton Beam Test at IUCF

One SEE test was performed on November 30, 2012 at IUCF with high-flux proton beams (Fig. 9). Three ADCs were irradiated with $\sim$ 200 MeV protons to measure SEU and SEFI (Single Event Function Interrupt) cross sections.

TABLE 2. SEE test results of three ADS5272 samples with 200 MeV proton beams

Samples	1	2	3
No. of SEFI	4	6	1
No. of SEE (single sample upset)	13	11	2
No. of SEE (Multiple sample upset)	0	2	0
Total	17	19	3
Fluence ($\times 10^{12}$/(cm^2 s))	5.01	4.70	3.02
Total beam-on time (s)	1848	1707	1117
Total ionization dose (kGy(Si))	3.00	2.81	1.81

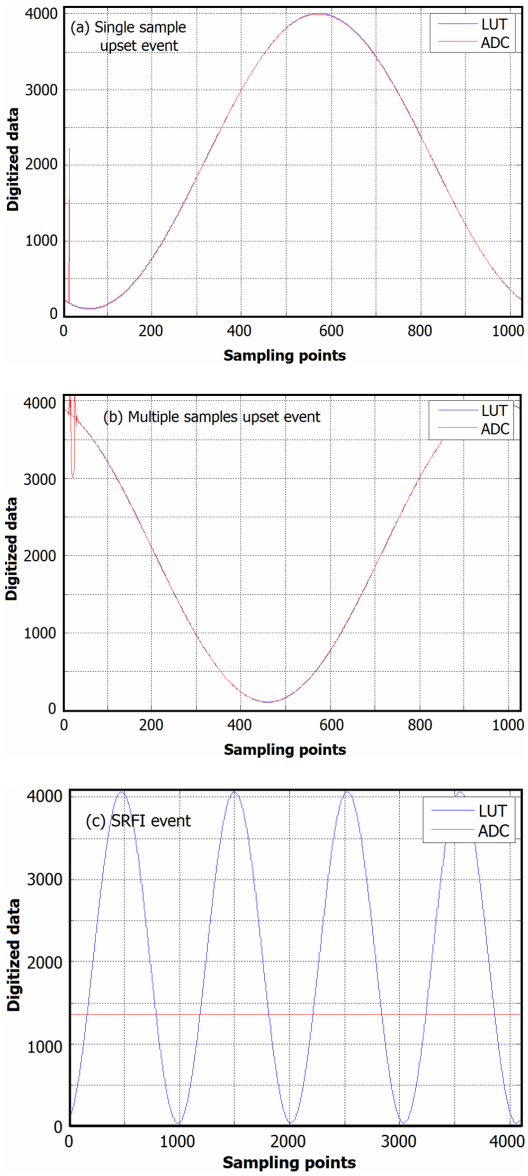

Fig. 10. (Color online) Graphical examples of SEU and SEFI . (a) Single sample upset event of ADC. Just a single sample off, but otherwise the ADC is working normally; (b) Multiple samples upset event of ADC, after that ADC recovered to normal working mode; (c) SEFI event of ADC, output is a constant value. The ADC recovered to normal working mode after hardware reset.

For the SEU (bit flip), the ADCs worked in no-external-intervention mode, i.e., with a single bit or multiple bits in the data stream flips, the ADCs continued to operate normally. Its impact was examined by the cross section measurements. SEFI was recorded when the ADCs ceased to operation: the ADC output remains constant, requiring an external reset to bring it back to normal mode. We note that the SEFI is not equal to a latch up as it does not need a power cycle for the ADC to recover. The ADS5272 could be reset in 200 ns without a power cycle.

Samples 1 and 2 were tested for cross section measurements without any special test conditions. Sample 3 was tested to evaluate the effectiveness of a mitigation strategy for SEFI and conditions modified to favor SEFI rather than detecting SEUs. A ~ 1 Hz hardware reset was issued to clear any register that might be corrupted by SEU outside of the data stream. Test results are listed in Table 2.

The total single event upsets (SEU) cross section is $\sigma_{\mathrm{SEU}} = (4.0 \pm 0.7) \times 10^{-12}\,\mathrm{cm}^2$. Although with poor statistics we observe that the upset probability is independent of the bit position in one ADC word (12bits). Therefore we specified SEU cross section in units of area per bit $\sigma_{\mathrm{SEU}}/\mathrm{bit} = (3.3 \pm 0.6) \times 10^{-13}\,\mathrm{cm}^2$. Graphical examples of SEU and SEFI are shown in Fig. 10.

V. CONCLUSION

In this paper, an evaluation system of ADS5272 has been established and its radiation performance has been characterized. From the irradiation test results, the ADS5272 performs very well up to 3 kGy (Si) TID and up to 5×10^{12} p/cm^2 fluence without significant performance degradation. These characteristics meet the radiation tolerance criteria of the COTS component for the LAr calorimeter front end (FE) electronics [1]. Therefore, the ADS5272 has been identified as a good candidate to be used in the future LAr calorimeter electronics upgrade, and a demonstrator LTDB is now being designed with this ADC. Valuable experience and information will be obtained from this demonstrator system after installing and running it at the high-luminosity of $L = 10^{34}/(\mathrm{cm}^2\,\mathrm{s})$ on the ATLAS LAr calorimeter.

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